AAT4686

OVPSwitch™

MOSFET Driver IC with Over-Voltage Protection

General Description

The AAT4686 OVPSwitch™ is a member of AnalogicTech's Application Specific Power MOSFET™ (ASPM™) product family. It is a P-channel MOSFET driver IC with precise over-voltage protection control, designed to protect low-voltage systems against high-voltage faults up to +28V. If the input voltage exceeds the programmed over-voltage threshold, the external P-channel MOSFET switch will be turned off to prevent damage to the output load circuits. The AAT4686 is available with an internally programmed over-voltage trip point or as an adjustable version programmed by a two external resistors.

The AAT4686 also includes an under-voltage lockout (UVLO) protection circuit, which will put the device into sleep mode at low input voltages only consuming < 1µA of current.

The AAT4686 is offered in a small Pb-free, 8-pin SC70JW package, and is specified for operation over the -40°C to +85°C ambient temperature range.

Features

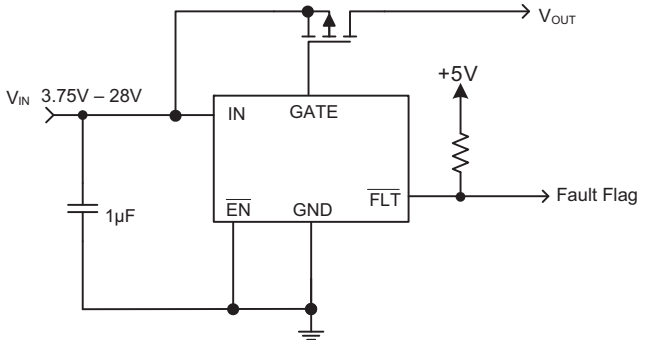
- Over-Voltage Protection up to 28V
- (Fixed or Adjustable) Over-Voltage Protection Threshold
- Fast OVP Response:
  - 1 µs (Max) to Over-Voltage Transient
- Low Operation Quiescent Current
  - 30µA Typical
  - 1µA Max in Shutdown (Disabled)
- Drives External P-Channel MOSFETs
- Under-Voltage Lockout
- Temperature Range: -40 to 85°C
- Available in SC70JW-8 Package

Applications

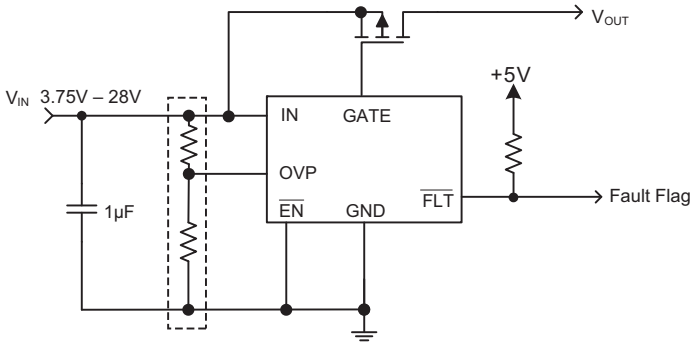
- Cell Phones
- Digital Still Cameras
- GPS
- MP3 Players
- Personal Data Assistants (PDA)
- USB Hot Swap / Live Insertion Devices

Typical Application

Fixed Version*



Adjustable Version



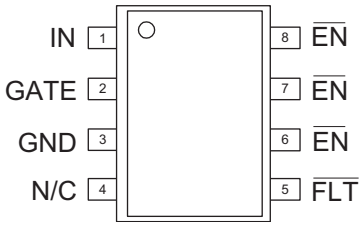
* Contact manufacturer for available options.

Pin Descriptions

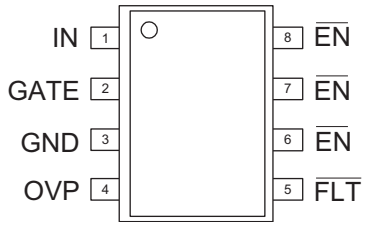
Pin #		Symbol	Function
Fixed	Adj.		
1		IN	Power input pin. Connect a 1µF capacitor from IN to GND.
2		GATE	Gate connection to external P-channel MOSFET.
3		GND	Ground.
N/C	4	NC/OVP	Fixed version: not connected. Adjustable version: Over-voltage protection threshold input.
5		$\overline{FLT}$	Over-voltage fault reporting.
6, 7, 8		$\overline{EN}$	Enable input, active low. When connected high, the device shuts down and draws less than 1.0µA of current. An internal pull-down resistor is connected to this pin.

Pin Configuration

Fixed OVP Trip Voltage Version SC70JW-8 (Top View)



Adjustable OVP Trip Voltage Version SC70JW-8 (Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	IN to GND	-0.3 to 28	V
V_{OVP}	OVP to GND	-0.3 to 6.5	V
$V_{\overline{FLT}}$, $V_{\overline{EN}}$	$\overline{FLT}$, $\overline{EN}$ to GND	-0.3 to 6.5	V
V_{GATE}	GATE to GND	28	V
T_J	Operating Junction Temperature Range	-40 to 150	°C

Thermal Characteristics

Symbol	Description	Value	Units
θ_{JA}	Maximum Thermal Resistance[2]	225	°C/W
P_D	Maximum Power Dissipation[2, 3]	440	mW

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a FR4 board.
3. Derated 4.4mW/°C above 25°C

Electrical Characteristics[1]

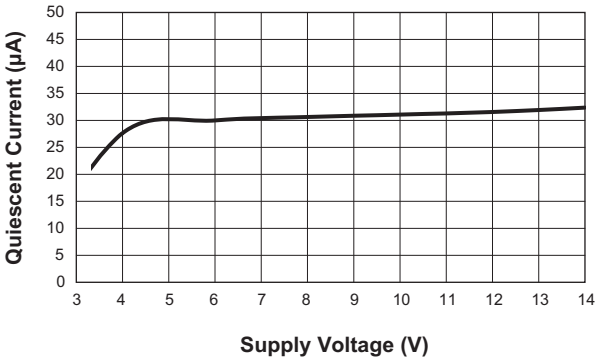
V_{IN} = 5V, T_A = -40° to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Normal Operation Voltage Range		3		14	V
I_Q	Operation Quiescent Current	V_{IN} = 5V, $\overline{EN}$ = 0V, I_{OUT} = 0		30	50	µA
$I_{SD(OFF)}$	Shutdown Supply Current	$\overline{EN}$ = IN, V_{IN} = 5.5V, V_{OUT} = 0			1	µA
V_{UVLO}	Under-Voltage Lockout Threshold	Rising Edge		3	3.3	V
V_{UVLO_HYS}	Under-Voltage Lockout Hysteresis			0.1		V
Adjustable						
V_{OVP_TH}	Over-Voltage Lockout Threshold, OVP Pin	Rising Edge	1.083	1.1	1.117	V
V_{OVP_HYS}	Over-Voltage Lockout Threshold Hysteresis, OVP			20		mV
Fixed						
V_{OVPT}	Over-Voltage Protection Trip Voltage	Rising Edge		6.5		V
V_{OVP_HYS}	Over-Voltage Protection Trip Point Hysteresis, IN Pin			120		mV
Gate Output						
V_{GHL}	Gate Voltage High Level	$\overline{EN}$ = V_{IN}	V_{IN}			V
V_{GLL}	Gate Voltage Low Level[2]			V_{IN} - 5V		V
I_G	Gate Current			1		µA
Logic						
$V_{EN(L)}$	$\overline{EN}$ Input Low Voltage				0.4	V
$V_{EN(H)}$	$\overline{EN}$ Input High Voltage		1.6			V
I_{EN}	$\overline{EN}$ Input Leakage	V_{EN} = 5.5V or 0V		0.5	2.0	µA
$\overline{FLT}_{OL}$	$\overline{FLT}$ Output Voltage Low	$I_{\overline{FLT}}$ = 1mA			0.4	V
$\overline{FLT}_{IOL}$	$\overline{FLT}$ Output Leakage Current				1	µA
T_{BLK_FLT}	$\overline{FLT}$ Blanking Time	From De-assertion of OV	5	10	15	ms
T_{D_FLT}	$\overline{FLT}$ Assertion Delay Time from Over-Voltage (OV)	From Assertion of OV		1		µs
T_{RESP_OV}	Over-Voltage Response Time	V_{IN} = 5V, V_{OVP} Rise to 1.13V from 1.07V in 1ns		0.7		µs
T_{ON}	Gate Turn On Delay Time	V_{IN} = 5V; C_G = 400pF		10		ms
T_R	Gate Turn On Fall Time	V_{IN} = 5V; C_G = 400pF		4		ms
T_{OFF}	Gate Turn Off Delay Time	V_{IN} = 5V; C_G= 400pF		6		ms

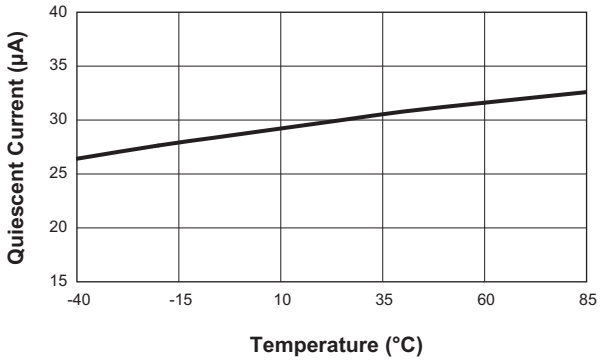
1. The AAT4686 is guaranteed to meet performance specification over the -40 to 85°C operating temperature range and are assured by design, characterization and correlation with statistical process controls.
2. V_{GS} (i.e. V_{IN_GATE}) is clamped to typical 5V.

Typical Characteristics

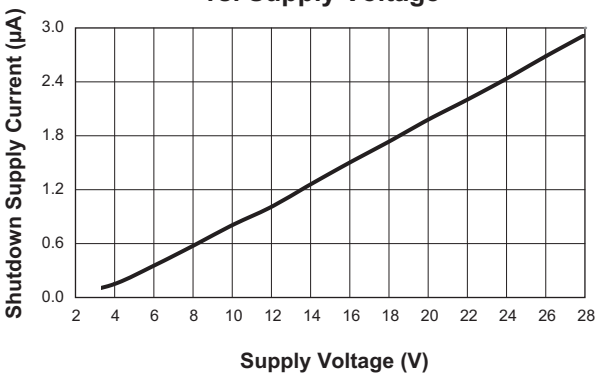
Operation Quiescent Current vs. Supply Voltage



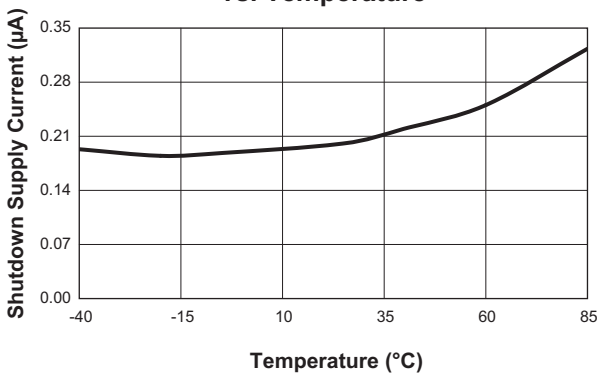
Operation Quiescent Current vs. Temperature



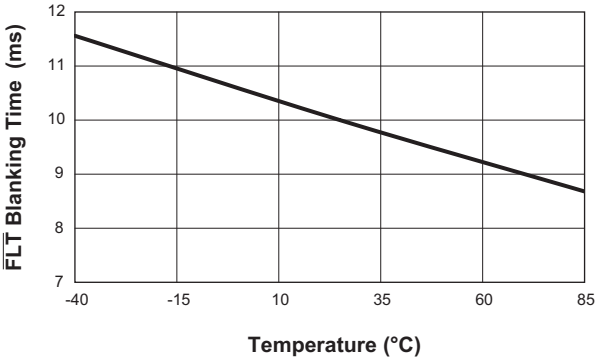
Shutdown Supply Current vs. Supply Voltage



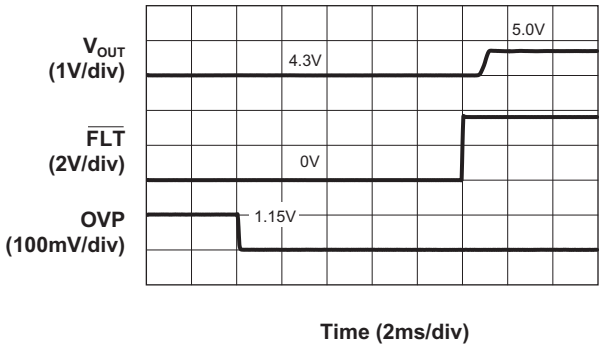
Shutdown Supply Current vs. Temperature



$\overline{FLT}$ Blanking Time vs. Temperature

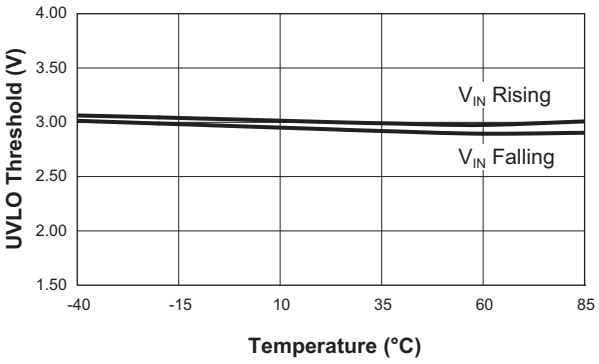


$\overline{FLT}$ Blanking Time
(V_{IN} = 5.0V)

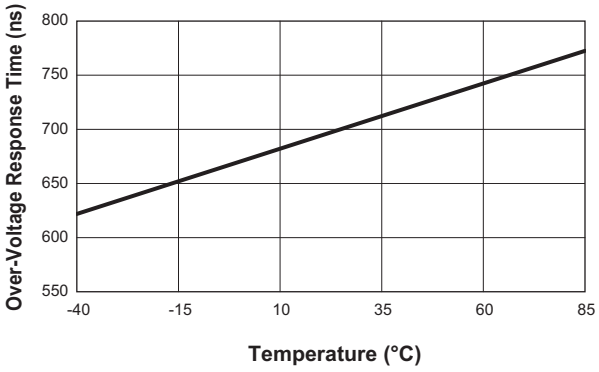


Typical Characteristics

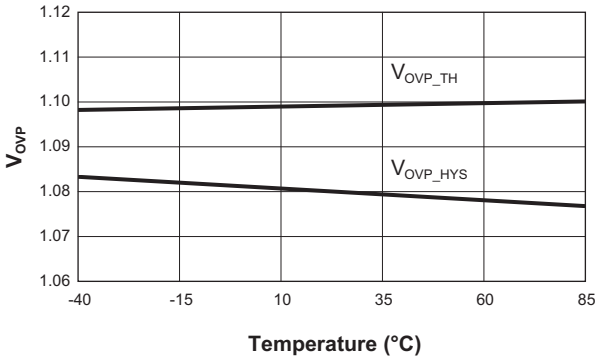
Undervoltage Lockout Threshold vs. Temperature



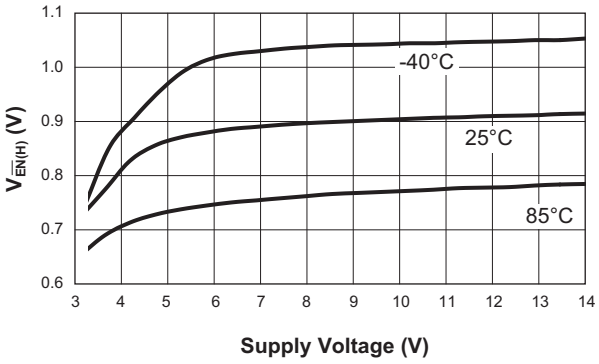
Over-Voltage Response Time vs. Temperature



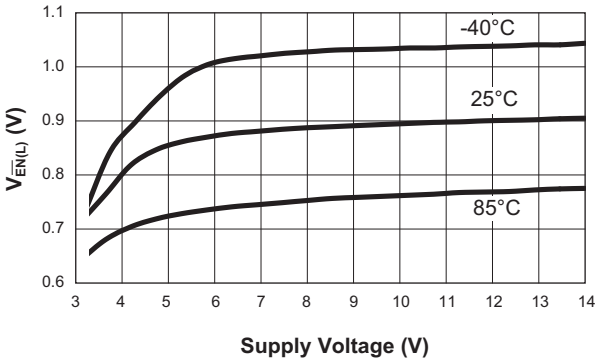
Over-Voltage Lockout Threshold (Adjustable Version) vs. Temperature



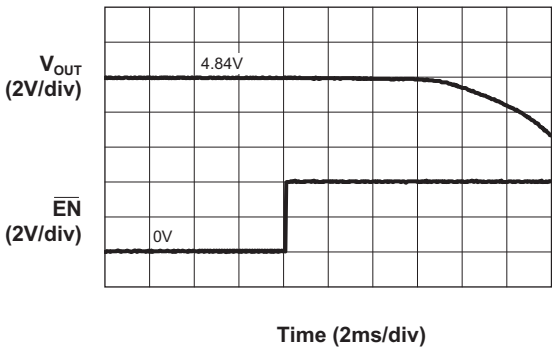
$\overline{EN}$ Input High Voltage vs. Supply Voltage



$\overline{EN}$ Input Low Voltage vs. Supply Voltage

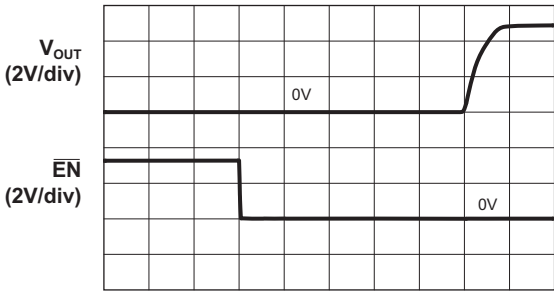


Turn Off Delay Time
(V_{IN} = 5.0V, R_O = 10Ω)



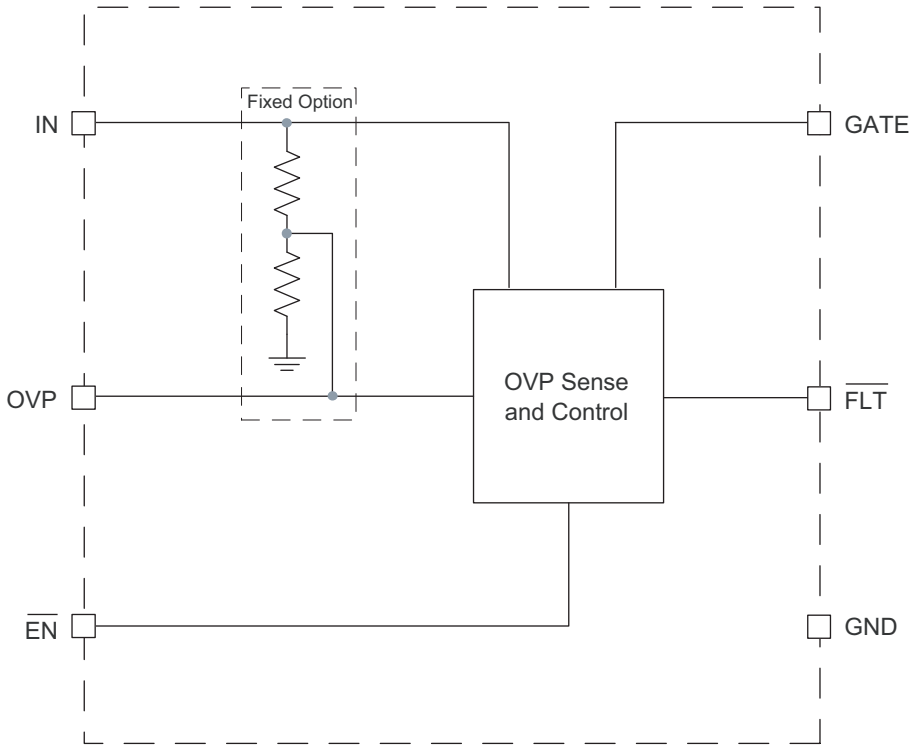
Typical Characteristics

Turn On Delay Time
(V_{IN} = 5.0V, R_O = 10Ω)



Time (2ms/div)

Functional Block Diagram



Functional Description

In conjunction with an external P-channel power MOSFET, the AAT4686 provides up to 28V over-voltage protection when powering low-voltage systems such as cell phones, MP3, and PDAs or when charging Lithium-Ion batteries from a poorly regulated supply. The P-channel MOSFET is inserted between the power supply or charger source and the load to be protected. The AAT4686 IC consists of a P-channel MOSFET slew-rate controlled driver, under-voltage lockout protection, over-voltage monitor, fast shutdown circuitry, and a fault output flag.

In normal operation, the P-channel MOSFET is controlled by the AAT4686, connecting and disconnecting the power supply from IN to OUT. A low resistance MOSFET is used to minimize the voltage drop between the voltage source and the load and to reduce the power dissipation. Any P-channel MOSFET can be used; however, the turn-on and turn-off speed will vary inversely proportionately to the MOSFET ON-resistance. When the input voltage exceeds the programmed voltage limit (internally set or externally by a voltage divider to the OVP pin), the device immediately turns off the external P-channel FET, disconnecting the load from the abnormal voltage and thus preventing damage to any downstream components. Simultaneously, the fault flag is raised, alerting the system to a problem.

If an over-voltage condition is applied at the time of the device enable, then the switch will remain OFF.

The AAT4686 can also be used as a simple slew-rate controlled P-channel high side driver IC.

Under-Voltage Lockout (UVLO)

The AAT4686 has a fixed 3.0V under-voltage lockout level (UVLO). When the input voltage is less than the UVLO level, the MOSFET is turned off. 100mV of hysteresis is included to ensure circuit stability.

Over-Voltage Protection

The AAT4686 adjustable version has a 1.1V ± 1.5% over-voltage trip threshold on the OVP pin. With a resistor divider on OVP pin from IN to GND, the over-voltage trip point can be adjusted anywhere within the input voltage range (see Table 1). Once the over-voltage trip level is triggered, the external PMOS switch controller will shut off the PMOS in less than 1µs.

The AAT4686 fixed version is also available with the resistor divider internally integrated and the input voltage trip point at 6.5V. The fixed version of the AAT4686 does not have a connection to the internal OVP circuitry and Pin 4 is designed to be not connected.

$\overline{\text{FLT}}$ Output

The $\overline{\text{FLT}}$ output is an active-low open-drain fault (OV) reporting output. A pull-up resistor should be connected from $\overline{\text{FLT}}$ to the logic I/O voltage of the host system. $\overline{\text{FLT}}$ will be asserted immediately if an over-voltage fault occurs (only about a 1µs inherited internal circuit delay). A 10ms blanking is applied to $\overline{\text{FLT}}$ signal prior to de-assertion.

$\overline{\text{EN}}$ Input

$\overline{\text{EN}}$ is an active-low enable input. EN is driven low, connected to ground, or left floating for normal device operation. Taking the $\overline{\text{EN}}$ high turns off the MOSFET. In the case of an over-voltage or UVLO condition toggling the $\overline{\text{EN}}$ will not override the fault condition and the switch will remain off.

Device Operation

On initial power-up, if V_{IN} < UVLO or if V_{OVP} > V_{OVP_TH} (1.1V), the PMOS is held off. If UVLO < V_{IN}, V_{OVP} < V_{OVP_TH}, and $\overline{\text{EN}}$ is low, the device enters startup after a 10ms internal delay.

Application Information

Over-Voltage Protection

The AAT4686 over-voltage protection circuit provides fast protection against transient voltage spikes and short duration spikes of high voltage from the power supply lines. The AAT4686 can quickly disconnect the input supply from the load and not cause any damage to sensitive components.

In portable product applications, if the user removes the battery pack during charging, this action can create large transients and a high voltage spike can occur which can damage other electronic devices in the product such as the battery charger. A hot plug of the AC/DC wall adapter into the AC outlet can create and release a voltage spike from the transformer. As a result, some sensitive devices within the product can be damaged. With the AAT4686 placed between the power lines and the sensitive devices, the voltage spike can be kept away and the input supply disconnected from other devices in 0.7µs.

Figure 2 shows the response time of over-voltage protection from the test circuit (Figure 1). The input voltage is rapidly increased from 5V to 12V by a voltage surge or voltage spike. The voltage at the OVP pin is also increased until the trip point is triggered. At this point, the $\overline{\text{FLT}}$ pin is pulled low and the output voltage starts to fall. Figure 3 shows a zoom-in scope capture of the OVP response time; the output is disconnected from the input in as little as 700ns.

Adjustable Version - Over-Voltage Protection Resistors

The over-voltage protection threshold is programmed with two resistors, R1 and R2. To limit the current going through the external resistor string while maintaining good noise immunity, use smaller resistor values, such as 10KΩ for R2. Using a larger value will further reduce the system current, but will also increase the impedance of the OVP node, making it more sensitive to external noise and interference.

$$V_{OVP} = V_{OVP\_TH} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

A suggested value for R2 is 110KΩ and R1 can be calculated from the following formula once the over-voltage protection voltage is set.

$$R_1 = R_2 \cdot \left(\frac{V_{OVP}}{V_{OVP\_TH}} - 1 \right)$$

Table 1 summarizes resistor values for various over-voltage settings. Use 1% tolerance metal film resistors for programming the desired OVP setting.

R2 (KΩ)	R1 (KΩ)	V_{OVP} Setting (V)
110	487	6.0
110	536	6.5
110	787	9.0
110	1050	11.5
110	1300	14.0
110	1540	16.5
110	1780	19.0
110	2050	21.5
110	2320	24.0
110	2550	26.5

Table 1: Recommended OVP Setting for AAT4686 Adjustable Version[1].

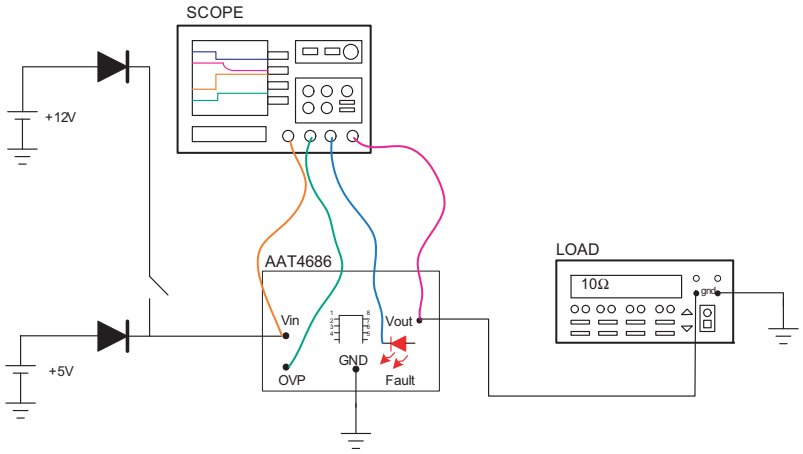


Figure 1: Over-Voltage Protection Response Time Test Circuit.

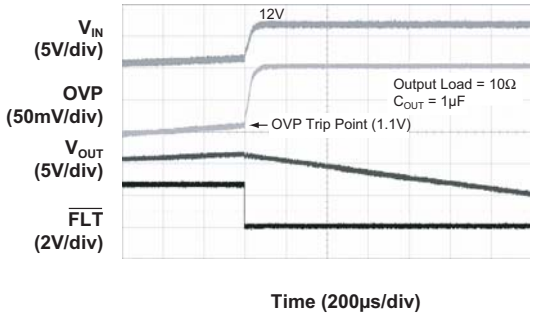


Figure 2: Typical Over-Voltage Response Time.

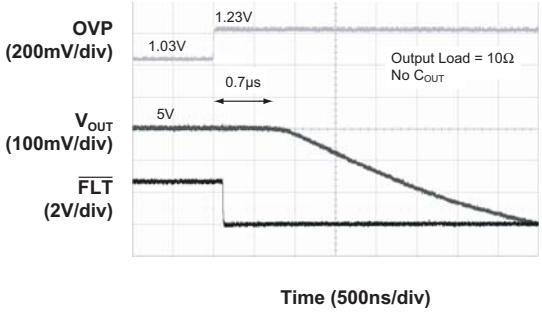


Figure 3: Typical Over-Voltage Response Time [zoom in].

1. Mimimum OVP voltage setting = 5V.

Input Capacitor

A 1µF or larger capacitor is typically recommended for C_{IN}. C_{IN} should be located as close to the device VIN pin as practically possible. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor equivalent series resistance (ESR) requirement for C_{IN}. However, for higher current operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Capacitors are typically manufactured in different voltage ratings. 16V, 25V, and 50V are good for OVP applications. If the maximum possible surge voltage is known, select capacitors with a voltage rating at least 5V higher than the maximum possible surge voltage. Otherwise, 50V rated capacitors are generally good for most OVP applications to prevent any surge voltage.

Output Capacitor

In order to insure stability while current limit is active, a small output capacitance of approximately 1µF is required at the output. Likewise, with the output capacitor, there is no specific capacitor ESR requirement. If desired, C_{OUT} may be increased to accommodate any load transient condition.

$\overline{\text{FAULT}}$ Flag

A $\overline{\text{FAULT}}$ flag is provided to alert the system if the AAT4686's input voltage has passed the pre-programmed over-voltage trip point. Since the $\overline{\text{FAULT}}$ is open drain pin, it should be pulled up to input/output voltage rail and less than the maximum operating voltage of 6.5V.

Thermal Considerations and High Output Current Applications

The AAT4686 is designed to deliver a continuous output load current. The limiting characteristic for maximum safe operating output load current is package power dissipation. In order to obtain high operating currents, careful device layout and circuit operating conditions must be taken into account. The following discussions will assume the load switch is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the "Printed Circuit Board Layout Recommendations" section of this datasheet. At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT4686 are maximum junction temperature ($T_{J(MAX)}$ = 125°C) and package thermal resistance (θ_{JA} = 225°C/W). Worst-case conditions are calculated at the maximum operating temperature, T_A = 85°C. Typical conditions are calculated under normal ambient conditions where T_A = 25°C. At T_A = 85°C, $P_{D(MAX)}$ = 175mW. At T_A = 25°C, $P_{D(MAX)}$ = 440mW.

The maximum continuous output current for the AAT4686 is a function of the package power dissipation and the R_{DS} of the MOSFET at $T_{J(MAX)}$. The maximum R_{DS} of the MOSFET at $T_{J(MAX)}$ is calculated by increasing the maximum room temperature.

For maximum current, refer to the following equation:

$$I_{OUT(MAX)} = \sqrt{\frac{P_{D(MAX)}}{R_{DS}}}$$

Printed Circuit Board Layout Recommendations

For proper thermal management, certain circuit board layout rules should be followed: VIN and VOUT should be routed using wider than normal traces, and GND should be connected to a ground plane. To maximize package thermal dissipation and power handling capacity of the AAT4686 SC70JW-8 package, the ground plane area connected to the ground pins should be made as large as possible. For best performance, C_{IN} and C_{OUT} should be placed close to the package pins; see Figures 4 and 5.

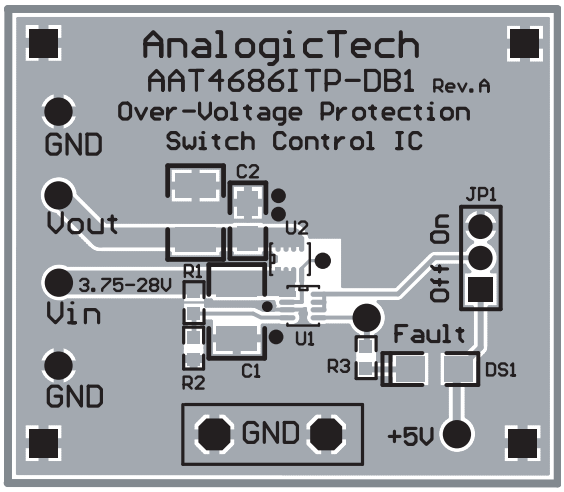


Figure 4: AAT4686 Evaluation Board Component Side Layout.

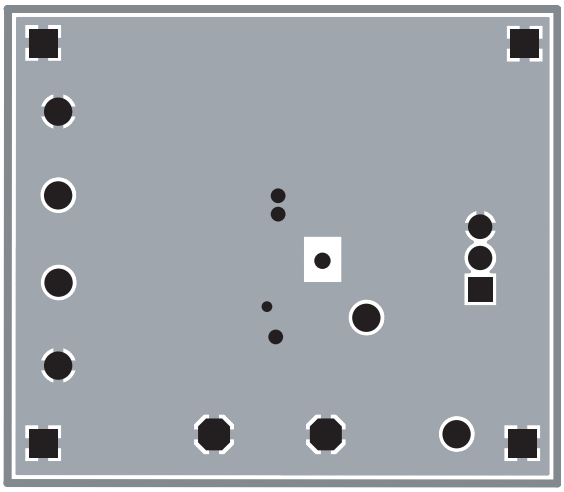
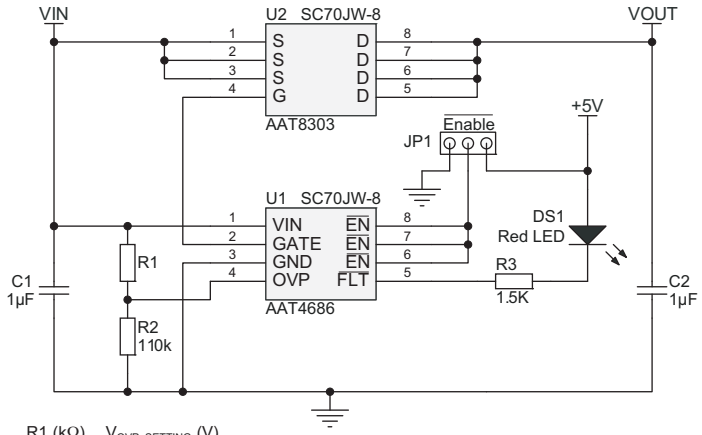


Figure 5: AAT4686 Evaluation Board Solder Side Layout.



R1 (kΩ)	$V_{OVP\_SETTING}$ (V)
487	6.0
536	6.5
787	9.0
1050	11.5
1300	14.0

Input Cap, C1
C1 1206 X7R 1µF 50V GRM31MR71H105KA88
(C1 1206 X7R 2.2µF 50V GRM31CR71H225KA88L)
(C1 1210 X7R 4.7µF 50V GRM32ER71H475KA88L)

Output Cap, C2
for under 13V application, C2 0805 X7R 1µF 16V GRM21BR71C105KA01
(for under 20V application, C2 0805 X7R 1µF 25V GRM219R71E105KA88)

Figure 6: AAT4686 Evaluation Board Schematic.

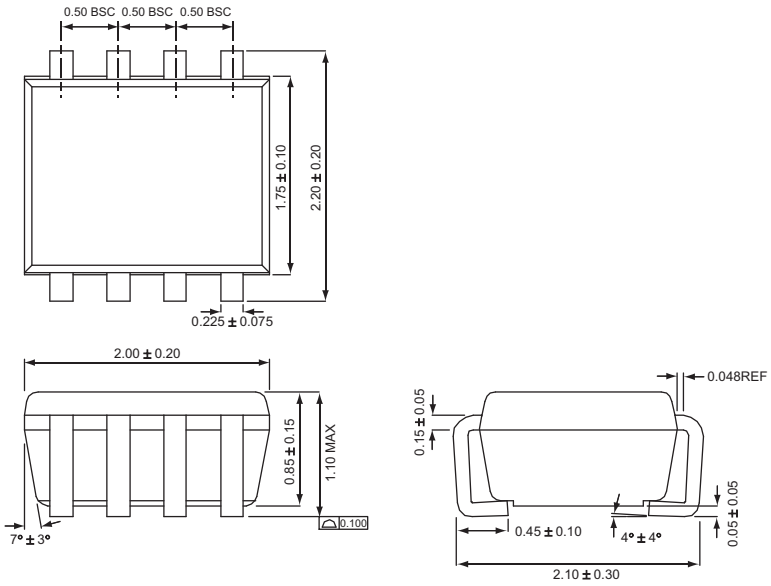
Ordering Information

Package	OVP Trip Voltage	Marking[1]	Part Number (Tape and Reel)[2]
SC70JW-8	Adjustable	YAXYY	**AAT4686IJS-T1**
SC70JW-8	6.5V		AAT4686IJS-6.5-T1

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Package Information

SC70JW-8



All measurements in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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